

BUILT-IN LOGIC BLOCK OBSERVATION TECHNIQUES

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Abstract

Parallel signature analysis with multiple-input signature registers allows to observe the data flow at internal testpoints on complex digital ICs. The test data are sampled and coded on-line at the rated internal speed of the ICs. The information about the data flow at the testpoints is gathered without putting an additional burden on the high speed data transfer between the ICs under test and the tester.

The feasibility of using parallel signature analysis for built-in test purposes is demonstrated by an example. Pseudorandom testpatterns generated with linear feedback shift registers are successfully used for detecting stuck-at faults in a bit-slice RALU circuit.

By adding a few gates to a multiple-input signature register, a multifunctional logic subsystem is obtained, which allows to combine the advantages of built-in test and scan path techniques.

Introduction

The generation as well as the application of production tests for today's highly complex digital integrated circuits are only manageable with a heavy support from extensive computer tools and costly automatic test equipment. And, the difficulties are growing at any further level of production: Several highly complex ICs are combined on a board to form a more complex circuit. The board itself is functionally and physically immersed into an even larger system. Once sold, this system gives rise to a new kind of problem: Neither the customer nor the maintenance and service persons are generally equipped with the vast technical support and the education, on which the manufacturers can base the production tests. This problem will even become more urgent in the future, since the low price and the virtually unlimited versatility of the modern microelectronic products will help to conquer new markets in up to now nonelectronic areas.

As a result, more and more very complex electronic products will be handled and maintained by nonprofessionals. Moreover, in some areas electronic control systems will substitute servomechanical devices in critical applications requiring a high reliability and safety.

These brief considerations reflect the fact that the problems associated with

- testing
- maintenance and service
- reliability and safety

will be a major challenge for the future development of microelectronic products. A decisive solution of these problems has to start at the IC level, since ICs are the basic building blocks of all modern microelectronic products. The most powerful method, being equally useful at all stages of the fabrication and life cycle of an electronic product, is to equip the ICs with test aids supporting a self-test of the products (Built-In Test).

So far, self test strategies have been mainly realized at the system level. Special IC designs supporting the self-test of systems have been successfully introduced only recently. Best known is the IC level implementation of scan path techniques in several large mainframe computers^{1,2,3}. The scan path provides an ideal interface for a maintenance and service processor, which itself is a part of the complete system. In this approach the diagnostic intelligence of the self-test is centralized in a dedicated module, namely the maintenance processor. In an alternative approach, the diagnostic intelligence is distributed over the system by implementing local test aids, which actively take part in the generation of testpatterns (i.e. input stimuli for the part of circuit under test), and/or the evaluation of testdata (i.e. answers at the outputs of the part of circuit under test). In a system level realization called Advanced Automatic Fault Isolation System (AAFIS)⁴ each subsystem (compartment holding several boards) contains a testpattern source, while the

evaluation of the testdata is done by a special circuitry on each individual board. The evaluation is performed by signature analysis in 9-bit serial signature registers, whose input can be successively connected with up to 32 individual testpoints.

In our own approach we propose an IC level implementation of signature analysis. A very effective and compact realization can be obtained by using multiple-input signature registers, which are discussed in section I. An example-demonstrating the feasibility of testing data path structures with built-in pseudorandom testpattern generation and multiple-input signature registers is outlined in section II. The ideas of scan path and signature analysis are combined in a special logic building block called BILBO, which is described in section III.

I. Multiple-Input Signature Registers

Digital circuits are tested by stimulating the inputs of the circuit under test with an appropriate sequence M_T of input words called testpatterns. T is the length of this sequence, i.e. the number of clock cycles needed to run the test. The circuit under test reacts to this stimulus by issuing a sequence Z_T of output words called testdata. Two things are necessary to happen for the detection of any hardware fault in the circuit under test: First, the fault has to be made visible at the outputs of the circuit under test. This is achieved, if, due to the fact that the fault is present, the testdata sequence Z_T issued by the circuit under test differs from the nominal sequence Z_T^n , that a faultfree circuit would have issued. The testpattern sequence M_T is responsible for doing this part of the job. In the second step, the fact that $Z_T \neq Z_T^n$ has to be registered and transformed into a fault message by some kind of testdata evaluating circuitry.

The quality of the test depends on both the quality of the testpattern sequence M_T and the quality of the testdata evaluating algorithm. Evaluating the testdata with a bit by bit comparison between Z_T and Z_T^n , like it is done in most automatic testers, is not suitable for an IC level implementation, since it generally requires a prohibitive amount of on-line memory containing the nominal sequence Z_T^n (stored response). However, there are several data compression techniques, which allow to compress the complete testdata sequence Z_T into a single codeword without losing too much information about eventual differences between Z_T and Z_T^n . A special type of codes, namely that of cyclic codes, is easily implementable with linear feedback shift registers⁵, and has been widely used since quite a time for error detection and/or error correction in data transmission

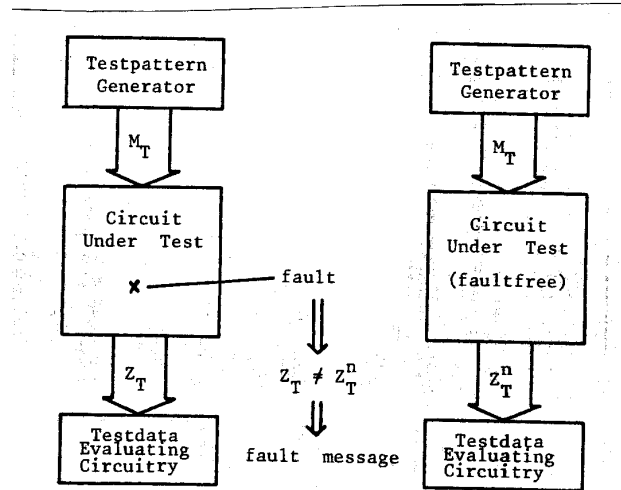


Figure 1: Fault detection in digital testing

applications. In the meantime, cyclic coding has also successfully entered the digital testing scene^{4,6,7}, where it is by now well known as signature analysis.

In adopting signature analysis for an IC level implementation, it is advisable to use parallel signatures rather than the serial signatures used in the above mentioned applications. This statement can be illustrated by the following example: Coding a sequence of 8-bit words with a serial signature would require either the parallel implementation of 8 serial signature registers (each serial signature register having only a single data input^{4,6}) or the implementation of a multiplexer, by which the input of one serial signature register can be successively connected to the 8 data lines⁴. Realizing the first of these suggestions would cost a prohibitive amount of chip area, while the second one would be time consuming by requiring at least 8 clock cycles to process a single 8-bit data word. Both difficulties can be overcome by using a multiple-input signature register as described by figure 2. At each clock cycle t a full data word $Z(t)=(z_1(t),z_2(t), \dots,z_8(t))$ can be entered into this kind of signature register via XOR-gates in all shift lines between the register cells. Thus, a complete sequence $Z_T = (Z(1),Z(2), \dots,Z(T))$ can be coded on-line within T clock cycles⁸.

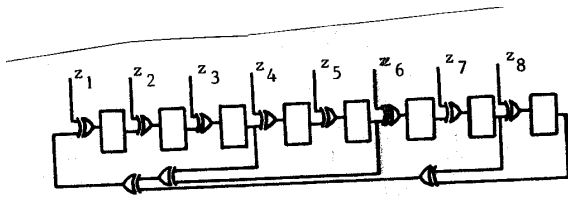


Figure 2: Multiple-input signature register for parallel signature analysis

Some basic features of multiple-input signature registers can be evaluated by exploiting their algebraic properties, especially their linear response with respect to XOR-operations in the data sequence Z_T to be coded. The key result for applications in digital testing is that an m -bit multiple-input signature register will registrate more than $100 \cdot (1-2^{-m})\%$ of all possible differences between the actually coded testdata sequence Z_T and the nominal sequence Z_T representing the faultfree case.

Before applying this result to real tests, an additional consideration seems to be worthwhile: The technologically induced physical faults and the actually used testpattern sequence M_T will generally excite only a small subset of all possible differences between Z_T and Z_T . It may therefore accidentally happen that this subset mostly contains differences, which are not registrated by the signature. In that case most of the faults will remain undetected. However, this mischief can be avoided with great likelihood, if the feedback tabs in the signature registers are arranged according to the prescriptions for obtaining pseudorandom sequences from linear feedback shift registers^{6,8}. The 8-bit signature register shown in figure 2 has this property: If all inputs z_1, \dots, z_8 are kept on fixed logical values, the register content will run through a pseudorandom sequence with maximum period length 2^8-1 .

II. Built-in Test with Multiple-Input Signature

Registers

Built-in multiple-input signature registers provide an excellent tool for monitoring internal testpoints on complex digital ICs. Together with on-chip testpattern generation a powerful method for a built-in test of internal logic blocks (modules) can be derived. An example is shown in figure 3.

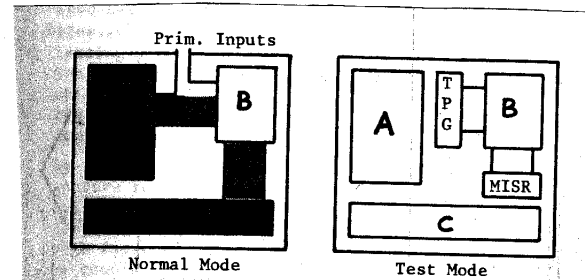


Figure 3: Built-in test for internal logic blocks on digital ICs

During normal mode operation, the logic block B is functionally embedded between the logic blocks A and C. Only the unshaded part of the inputs of B can be directly controlled from primary inputs of the chip. None of the inputs of B can be directly observed at the primary output lines of the chips. In a special testmode, the inputs of B are connected to a built-in testpattern generator (TPG), while the outputs of B are monitored by a multiple-input signature register (MISR). The choice of an appropriate testpattern generation algorithm depends on the type of logic block to be tested. However, one has always to keep in mind that the overhead (software, firmware or hardware) needed for implementing the TPG has to be kept minimal. This can be achieved by using parts of the normal logic, wherever possible. If B for instance is a microcode ROM on a microcomputer, the program counter running through the entire address space of the ROM may be used as a hardware TPG during the test mode operation. Some other types of tests, like those for RAMS, are most effectively implemented in firmware or software.

Pseudorandom testpatterns are well suited for a hardware implementation with linear feedback shift registers⁹. The effectivity of pseudorandom patterns for testing combinational circuits have been investigated both theoretically¹⁰ and experimentally¹¹, and the experiences made with AAFIS show that, at least within limits, pseudorandom testing may also be successful for testing sequential circuits⁴. These results have been confirmed by

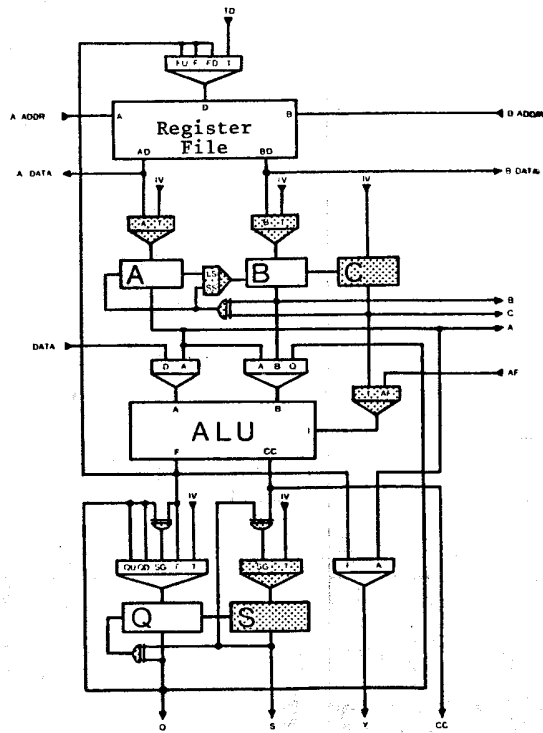


Figure 4: Logic block diagram of a bit-slice processor with built-in test capabilities.

our own experiments¹². Figure 4 shows the logic block diagram of the TTL breadboard model used in the experiments. Built-in test capabilities are realized by adding the shaded components to an existing bit-slice circuit. During the test mode operation, the latches A, B and C are functionally converted into a 12-bit pseudorandom TPG serving the two 4-bit operand inputs (A, B) and the 4-bit function select input (I) of the ALU. The registers Q and S are converted into an 8-bit multiple-input signature register monitoring the 4-bit result (F) and the 4-bit status output (CC) of the ALU operation. In a second test mode only 8 bits of the pseudorandom TPG are used for stimulating the B and I inputs of the ALU, while the second operand A is extracted from the register file, which intermediately stores the results of previous ALU operations. Thus, two types of built-in test are realized in the model. (cf. Figure 5).

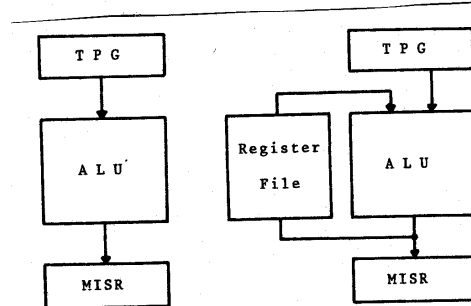


Figure 5: Test modes

During the experiments up to 40 different stuck-at faults were physically inserted at the IC pins of the breadboard models. All simulated faults were detected by the pseudorandom testpatterns and the parallel signatures after only 30 clock cycles. The set of simulated faults also included faults at the pins of the TPG and the MISR. More extensive gate level fault simulations with up to 900 different internal stuck-at faults were run on a minicomputer.

The results of the simulation runs show that pseudorandom testpatterns are effective for testing data path structures like the ALU subsystems of microcomputers. The fault detection effectivity decreases^{10,11}, if gates with extremely high fan-in are used in the design of the data path. Thus, the method. is best suited for testing circuits, which are designed in random logic with low average fan-in. As has already been mentioned above, different methods of testpattern generation may be used for other circuit types. However, parallel signature analysis with multiple-input signature registers works in any case.

III. BILBO

The experiences made with pseudorandom testpatterns and multiple-input signature registers stimulated the development of a multifunctional subsystem called Built-In Logic Block Observer (BILBO13), which can be used for data transfer and fault detection purposes in complex digital circuits.

Each BILBO is composed of a flipflop register row and some additional gates for shift and feedback operations (cf. figure 6). Four different functional modes can be selected by setting two control inputs, B1 and B2.

In the first mode (B1=1, B2=1), BILBO acts as a latch. The input data z_1, z_2, \dots, z_8 are simultaneously clocked into the flipflops and can be read from the Q and Q outputs.

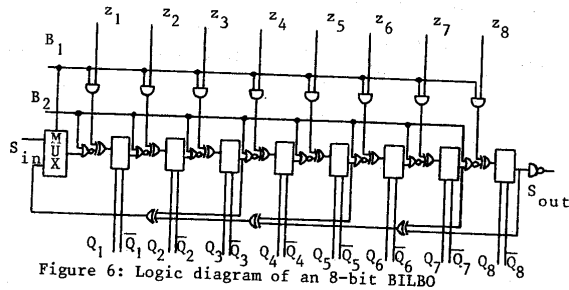


Figure 6: Logic diagram of an 8-bit BILBO

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In the second mode ($B_1=0, B_2=0$), BILBO works as a linear shift register. Data are serially clocked into the register through the serial input S_{in} , while the register contents can be simultaneously read at the parallel Q and \bar{Q} outputs, or can be clocked out through the serial output S_{out} . The shift register feature of BILBO may be utilized both in the normal mode and in a test mode. In the latter mode BILBO may for instance become a part of a scan path.

In the third mode ($B_1=1, B_2=0$) BILBO is functionally converted into a multiple-input signature register like that shown in figure 2. As has already been discussed in section I, in this mode BILBO may be used for performing parallel signature analysis or for issuing pseudorandom sequences. The latter application is achieved by keeping the inputs z_1, z_2, \dots, z_g on fixed logical values. The remaining fourth mode ($B_1=0, B_2=1$) forces a reset on the register.

The versatility of BILBO allows to combine the advantages of built-in test at the rated internal speed of the ICs and the high fault resolution quality of scan-path techniques. Figure 7 shows a possible way for using BILBOs in a modular bus oriented design. First, the scan path mode may be used for initializing the system, if no other reset modes are available. Then the system is switched to a self-test mode utilizing pseudorandom testpatterns and parallel signature analysis for a previously specified number of clock cycles. The resulting signatures, which contain eventual fault messages, can be clocked out after switching back to the scanpath mode. The scan-path mode can also be used for the detection of faults, which are not efficiently detected by the self-test, or for a gate-level diagnosis in order to reveal design and technology problems. During the normal mode operation the BILBOs can be used as latches and/or shift registers.

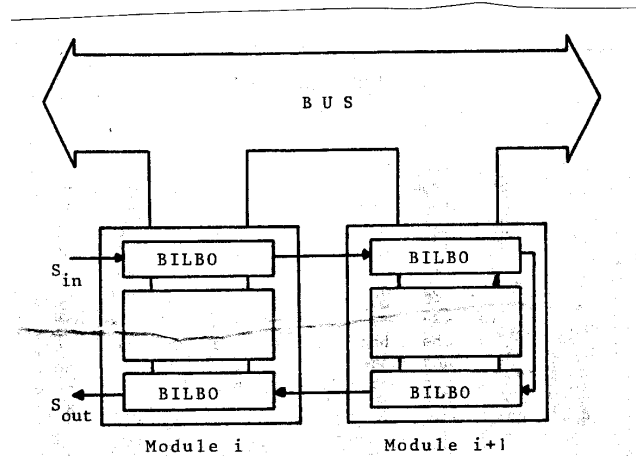


Figure 7: Modular bus-oriented design with BILBOs

Conclusions

The multiple-input signature registers described in section I are very efficient and compact tools for monitoring internal testpoints on complex digital ICs. Any deviations from the nominal data sequence (representing the faultfree case) at the testpoints are registered by an m-bit signature with a security of more than $100(1-2^{-m})\%$. The data sampling and coding is performed at the internal rated speed completely inside the ICs. Thus, monitoring internal testpoints with multiple-input signature registers does not put an additional burden on the highspeed data transfer between the ICs and an external tester. The information about the logical behavior of internal testpoints is obtained without using time consuming procedures like multiplexing or serially shifting the data out of the chips.

If combined with on-chip testpattern generation, parallel signature analysis with multiple-input signature registers provides a powerful tool for implementing a built-in test for internal logic blocks. Due to the possibility of gating the internally generated testpatterns to appropriate internal circuit nodes, it becomes feasible to use relatively simple testpattern generators even for testing parts of very complex circuits. Pseudorandom testpatterns generated with linear feedback shift registers are thus efficiently usable for testing internal data path structures like the RALU component of a microcomputer.

By adding only a few gates to a multiple-input signature register, a multifunctional logic subsystem called BILBO is obtained. With the help of BILBO, the advantages of a highspeed built-in test and the high fault resolution of

scan path techniques can be combined to perform a thorough and yet simple test of VLSI chips.

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